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Design & Analysis of Mixed-mode Integrated Circuit for Pulse-shape Discrimination

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by

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I would first like to thank my family for their support during all of my higher education pursuits. I could not have come this far without them.

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Bryan Orabutt

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Dedicated to my mother Marsha and brother Sean for sticking with me through all of my educational pursuits.

ABSTRACT OF THE THESIS

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Research Advisor: Professor Roger Chamberlain

Abstract: In nuclear science experiments it is usually necessary to determine the type of radiation, its energy and direction with considerable accuracy. The detection of neutrons and discriminating them from gamma rays is particularly difficult. A popular method of doing so is to measure characteristics intrinsic to the pulse shape of each radiation type in order to perform pulse-shape discrimination (PSD).

Historically, PSD capable systems have been designed with two approaches in mind: specialized analog circuitry, or digital signal processing (DSP). In this work we propose a PSD capable circuit topology using techniques from both the analog and DSP domains. We call this circuit topology a mixed-mode PSD system. We model this mixed-mode PSD system using Verilog-A and simulate its performance using Cadence Spectre with real detector waveform data as the input. We show that our mixed-mode PSD system is capable of discriminating between neutrons and gamma rays at least as well as state of the art DSP based systems while offering some of the advantages of both analog based and DSP based systems.

Chapter 1

Introduction

The ability to distinguish between multiple kinds of radiation is a necessity in many nuclear science experiments. Gamma rays and neutrons are often very difficult to distinguish between which has led to high demand for specialized electronics capable of discriminating between them. Additionally, position determination often requires detector arrays with many (even thousands) of elements. A common technique for discriminating between radiation types is known as pulse-shape discrimination (PSD). In analog based systems an analog application specific integrated circuit (ASIC) does most or all of the pulse processing on chip [4], providing two or three sample points that are digitized and analyzed offline. The biggest issue with this approach is that analog ASICs are algorithm locked which limits the ability of a researcher to do any additional analysis, error correction algorithms, or different discrimination algorithms. The advantage is that analog ASICs often support many channels [5] and are very inexpensive which is useful for large detector arrays with thousands of channels.

Another approach to PSD is to use digital signal processing (DSP). For this method fast sampling (on the order of 100 MSPS or more) analog-to-digital converters are used to fully sample the entire detector pulse waveform. Since there are enough data points to get a clear picture of the wave shape it allows for many different algorithms to be used that can help correct errors, correlate events, or just give a more accurate discrimination result [17]. The major disadvantage of DSP based systems is that they rely on fast digitizers to get enough time resolution in the sampled waveform for doing PSD [2]. Digitizers fast enough to do PSD are cost prohibitive for use in detector arrays with more than a few dozen channels.

In this work we propose a middle ground between these two methodologies. In our mixed-mode PSD system we do some of the pulse processing on chip via analog circuits, however we

store intermediate samples on chip in analog memory. This allows the ASIC to have many channels since the circuitry is relatively simple, but also allows for slow digitizers to be used since samples are held on chip until they have been successfully digitized. We show that this is a viable technique for implementing a PSD capable ASIC by modeling our circuit topology in Verilog-A. We use real detector waveform data from multiple scintillators as the input to our system models and compare it with results from other works using DSP techniques.

The outline of the thesis is as follows. Chapter 2 introduces background knowledge including how PSD works and other works that have attempted to make PSD capable systems. Chapter 3 describes our mixed-mode system in detail. Chapter 4 shows the simulated results of our mixed-mode system and compares them with results of the state of the art. Chapter 5 draws the conclusion for the viability of a mixed-mode PSD system and elaborates on future work that could enhance the work presented in this thesis.

The results of this work have been published [13]. The code and Cadence project files are available at [11] and [12].

Chapter 2

Background and Related Work

The most common class of neutron detectors are organic scintillators and as a result most PSD capable systems are designed with these scintillators in mind. The high hydrogen content enhances the probability of generating recoil protons. The ionization generated by these recoil protons is more dense than that generated by the gamma-ray generated electrons from either the photoelectric effect or Compton scattering. Both recoiling protons and electrons generate copious amounts of excited molecular singlet (S^*) and triplet (T^*) states. The singlet states decay quickly (some 10's of ns) while the triplet states, where they do decay via their natural lifetime, would be so slow to be uncorrelatable to the nuclear event generating the radiation. ($T \rightarrow S$, is a forbidden electromagnetic transition.)

The basis of n/γ discrimination lies in an enhanced probability that the higher density of ionization from the recoiling protons generates a significant probability of what is triplet annihilation, i.e. $T^*+T^* \rightarrow S+S^*$. The excited singlet can then emit a photon. These photons are delayed relative to those that result from the de-exciting singlets directly produced by the incoming radiation by the time the excitation energy was sequestered in the triplet states [7]. Techniques for analyzing the output waveform (pulse shape) from scintillators to extract the form of the impinging radiation are called pulse-shape discrimination. Pulse-shape differences are modest and can be lost by poor pulse processing techniques or small energy deposition in the scintillator.

Figure 2.1 shows an experiment employing PSD. An ion beam is pulsed on for a brief duration and strikes a target. This is repeated in regular intervals with each period referred to as a beam dump. Each beam dump causes radiation to shower onto a wall of scintillator detectors which are used for PSD. The scintillators are coupled to a transducer, either a

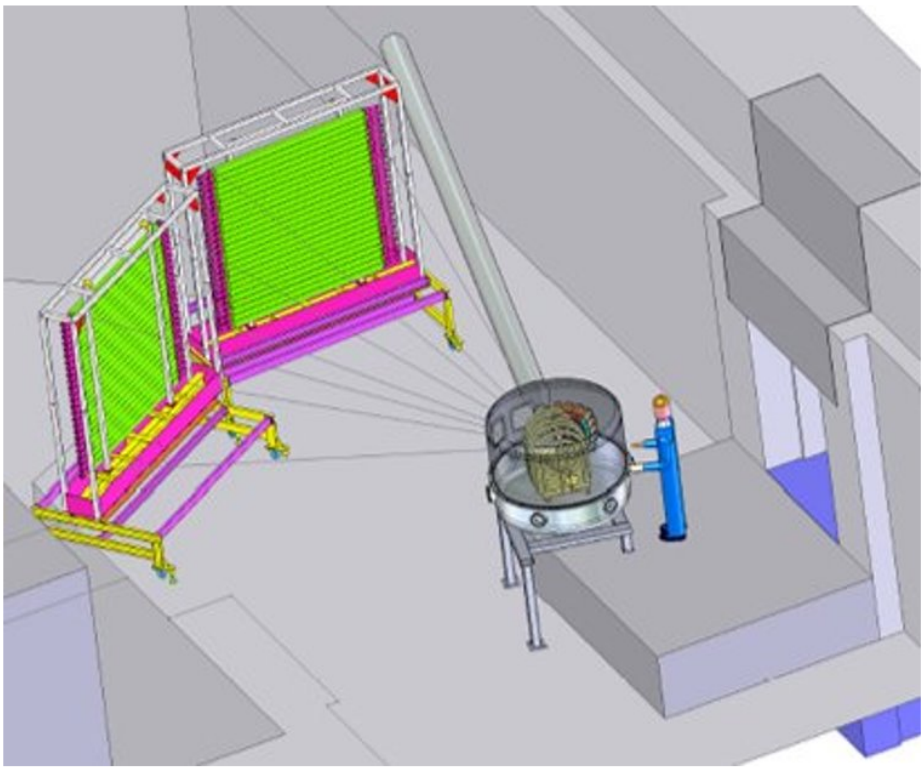

Figure 2.1: A typical experiment employing PSD.

photo multiplier tube (PMT) or photodiode, which converts the light output into an electrical signal. The electrical signals are then processed by the pulse processing electronics, which may be analog or DSP based.

PSD relies on the fact that gamma rays and neutrons have a small, but predictable, difference in their pulse shape at similar energies. Figure 2.2 shows two pulses from [18], one from a neutron and the other from a gamma ray, as recorded by the light generated by a common organic scintillator. There are many PSD techniques for quantifying the difference between gamma rays and neutrons but the most common is the charge comparison method (CCM). In this method two integration regions are chosen, typically some region in the pulse tail and the entirety of the pulse. A discriminating parameter, D, is then defined as

$$D = \frac{\int_{t_1}^{t_2} Q dt}{\int_{t_0}^{t_2} Q dt} \tag{2.1}$$

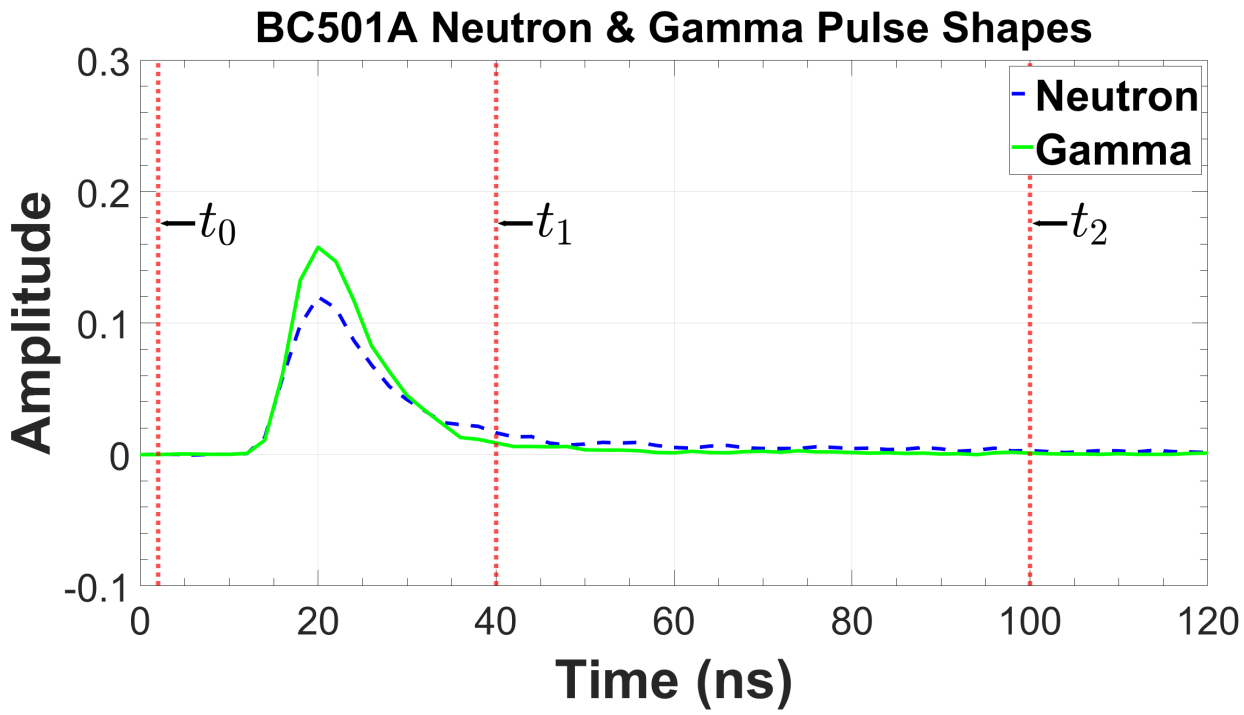

Figure 2.2: n/γ waveforms from a BC501A scintillator. The time of t_2 is taken as 100 ns for illustration purposes. The actual total integration gates are several hundred nanoseconds.

where the time range t_0 to t_2 is the total integration gate which covers the pulse in its entirety, and the time range t_1 to t_2 is the pulse tail region. Because a gamma ray of similar energy from an identical scintillator will always have a faster decay time, D will be larger for neutrons than it is for gamma rays. Thus when plotting D vs radiation energy, as shown in Figure 2.3, a bimodal distribution is formed with gamma rays and neutrons being separated.

There are several existing works which aimed to create systems that are PSD capable. One of which is the PSD8C ASIC developed in the VLSI design lab at Southern Illinois University Edwardsville [6][14]. PSD8C is an analog ASIC capable of supporting up to eight detector channels on a single chip [5]. Figure 2.4 shows a typical system employing the PSD8C ASIC. The PSD8C chip employs CCM to discriminate between neutrons and gamma rays. It does so by using hardware integrators on chip that can be pre-programmed with different integration gate delays and gate widths. An external constant fraction discriminator is used to start the gated integrators which then compute the integrals over different regions of the

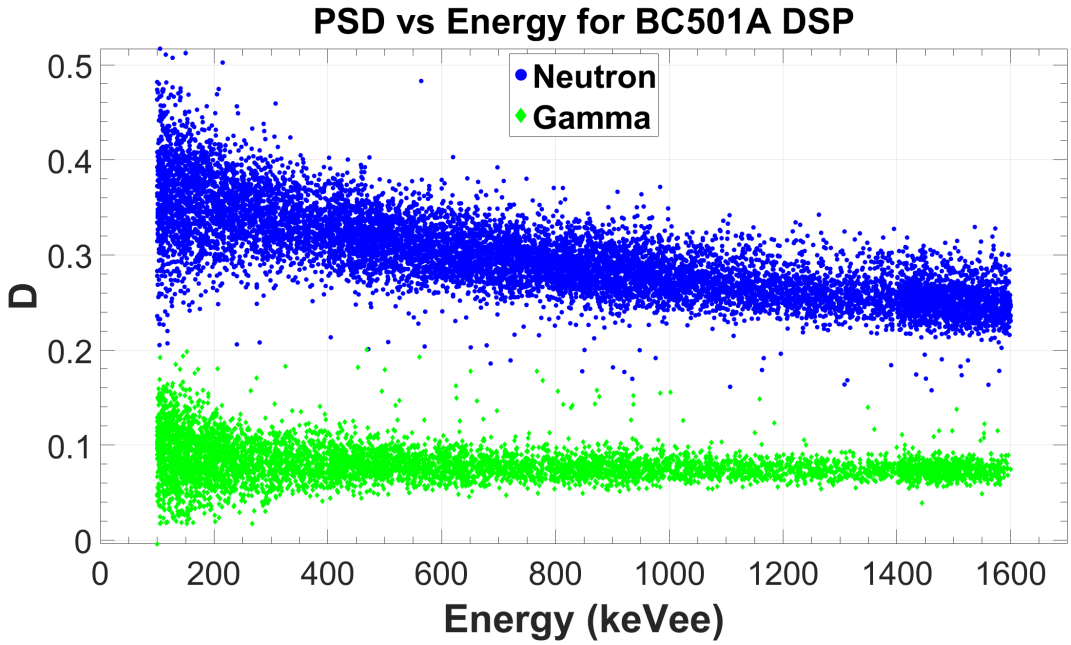

Figure 2.3: n/γ discrimination in BC501a using traditional DSP methods. The units keVee are keV-electron-equivalent which describes the light output of the scinitllator with respect to the light output of an electron at a given energy. This gives a common comparison unit since electrons (gamma) and neutrons will give different light outputs for the same energy deposited.

pulse giving three sample outputs per channel. These samples are digitized and their ratios taken to create a discriminating variable using the definition given in equation 2.1.

There are some drawbacks to this design however. If an integrator saturates it is impossible to know when the saturation occurred. If it happened at the very end of the integration period then the sample should still be used, however if it saturates early on it needs to be thrown out and that pulse data can not be analyzed. Since it is impossible to determine which scenario happens all saturated integrals will result in pulse data being thrown out and unused. Another issue is that if multiple events occur close temporally on the same channel, a condition known as pileup, it is impossible to detect since the chip only provides three data points making the detector wave shape impossible to recover.

Another work that did not explicitly have PSD as a design goal but was a heavy influence in some of the design decisions in our mixed-mode topology is the DRS4 ASIC. The domino ring sampler 4 (DRS4) ASIC is a high speed pulse sampling circuit capable of sample rates

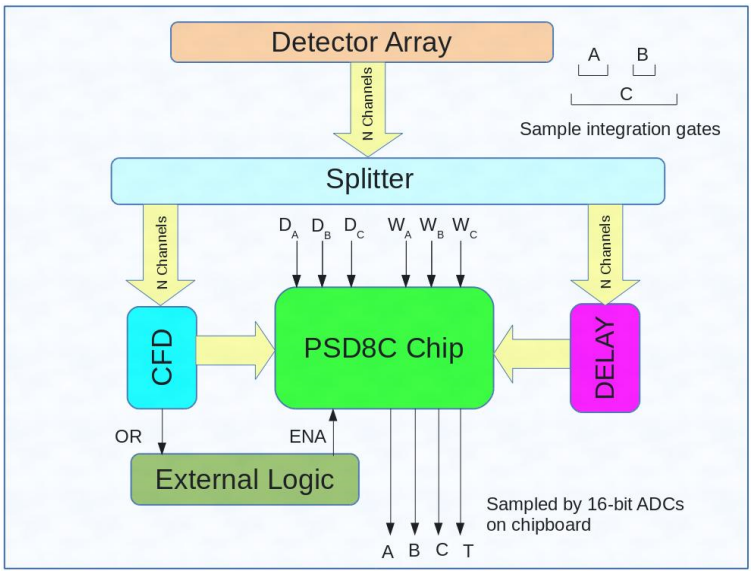

Figure 2.4: A typical PSD8C system. A detector output is split to align the detector pulse with a constant fraction discriminator signal used to start integration.

up to 6 GHz [15]. The DRS4 (shown in Figure 2.5) can support up to eight detector channels, similar to PSD8C. Each detector channel is composed of a long chain of 1024 sampling capacitors. On the rising edge of each sample clock a voltage sample is stored on one of these capacitors. After an external trigger signal is applied all channels stop sampling allowing the individual capacitor samples to be digitized by an off chip analog to digital converter (ADC).

The DRS4 has many great features that would make it a good candidate ASIC for PSD applications. There are some drawbacks that make it not ideal for our target applications however. The DRS4 can only operate between 500 MHz and 6 GHz. Since each clock cycle a sample is stored on a capacitor this limits the total time range that can be stored on chip to between 170 ns and 2 μs. For fast scintillators this is not an issue, however some slower scintillators might need integration gates that are several microseconds wide. This can be overcome by cascading DRS4 channels, however this means fewer detector channels per chip and thus more chips needed which mitigates the cost benefits of the ASIC. Another issue is that the trigger signal on the DRS4 is global, stopping all channels in response to a signal trigger. Ideally channels should be individually triggered to give the lowest probability of missing an event during a beam dump.

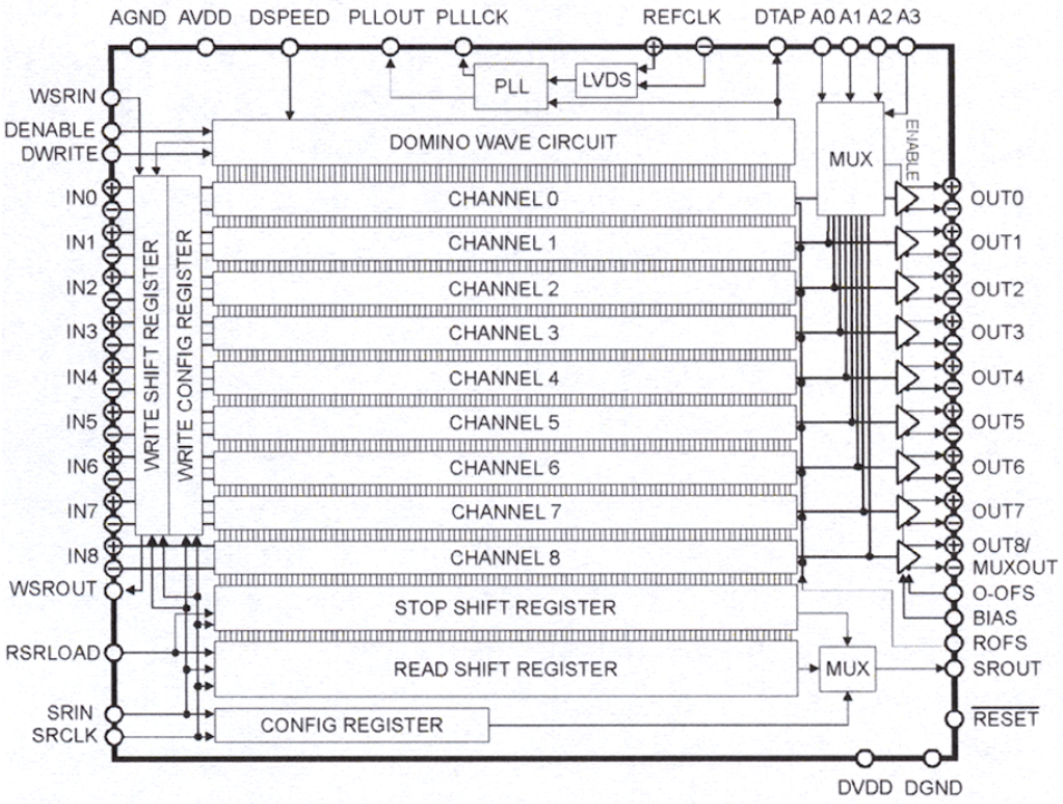

Figure 2.5: The domino ring sampler 4 ASIC block diagram.

Other work has also been done to make cost effective DSP based systems that can be deployed on large channel count detectors. One such method takes advantage of the fact that the majority of the differences between γ-ray and neutron pulse shapes exists in the pulse tail. Since the pulse tail decays very slowly it contains frequency components mostly at very low frequencies (see Figure 2.6). To take advantage of this frequency domain PSD algorithms can be used instead of time domain, coupled with slower more inexpensive ADCs. This concept is explored in [9] to great effect, showing that slow digitizers can still give good discrimination properties for PSD.

There are a few downsides to this approach that must be considered. If low sample rate ADCs are used then frequency domain algorithms *must* be employed. Figure 2.7 shows that when using slow ADCs, samples do not necessarily align well with the total and tail gates. This leaves significant time domain pulse-shape information lost making performance poor [9]. This means traditional time domain algorithms for PSD, pileup detection, and

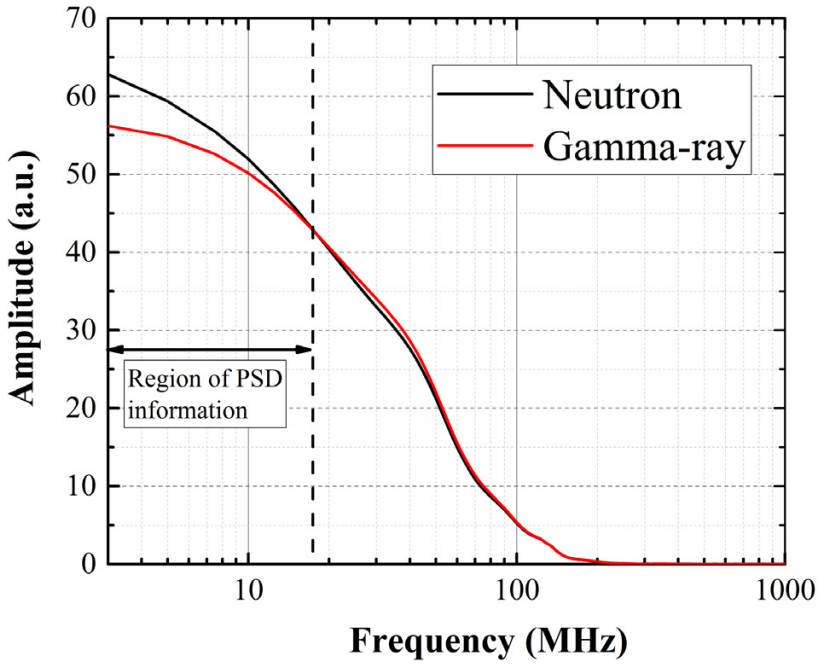

Figure 2.6: As can be seen, the majority of the differentiating components between γ-rays and neutrons is contained below 18 MHz [9].

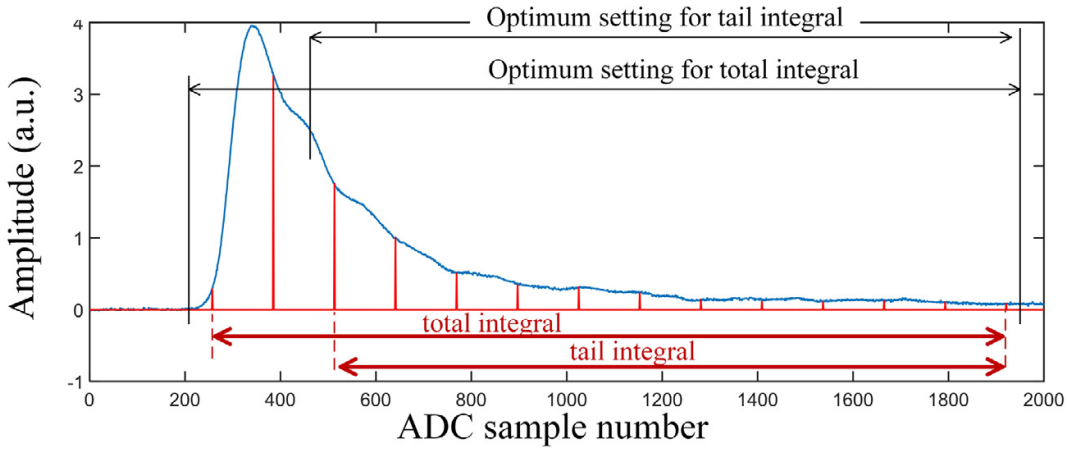

Figure 2.7: Using low sample rates to do PSD means significant portions of the pulse content might exist outside of the optimal range reducing PSD performance using time domain algorithms [9].

error correction cannot be employed. Another issue that the low sample rate ADCs may not accurately resolve the pulse peak. While these issues may not be important if radiation

discrimination is all that is required, there are many applications where pulse height is important [3].

Chapter 3

System Architecture & Modeling

3.1 System topology

Our proposed mixed-mode PSD system, shown in Figure 3.1, is a multi-channel system capable of supporting multiple detector channels on a single chip. The input to each detector channel is a hardware integrator, the output of which is sampled periodically. The samples are stored in sample and hold units (S&H) which allows the integral samples to be digitized later rather than immediately when the pulse comes through. This allows the use of digitizers much slower than would typically be used for DSP, but still gives many samples as an output to allow for DSP algorithms to be utilized.

3.1.1 Detector Channel

Each detector channel is separated into a high-gain and low-gain sub-channel for dynamic range enhancement. Aside from the gain on the integrators the sub-channels are functionally identical. Immediately following the integrators is a short block of analog memory formed from sample and hold units called the short buffer. This short buffer is an analog ring buffer where samples are continuously stored on the rising edge of every clock cycle until the channel gets a trigger signal. After a CFD trigger indicates pulse data is available in the short buffer, an additional k samples will be saved into the short buffer, where k is determined by the scintillator's optimal slow integration gate [18]. Once these k samples are saved, the system begins sampling into an available long tail buffer.

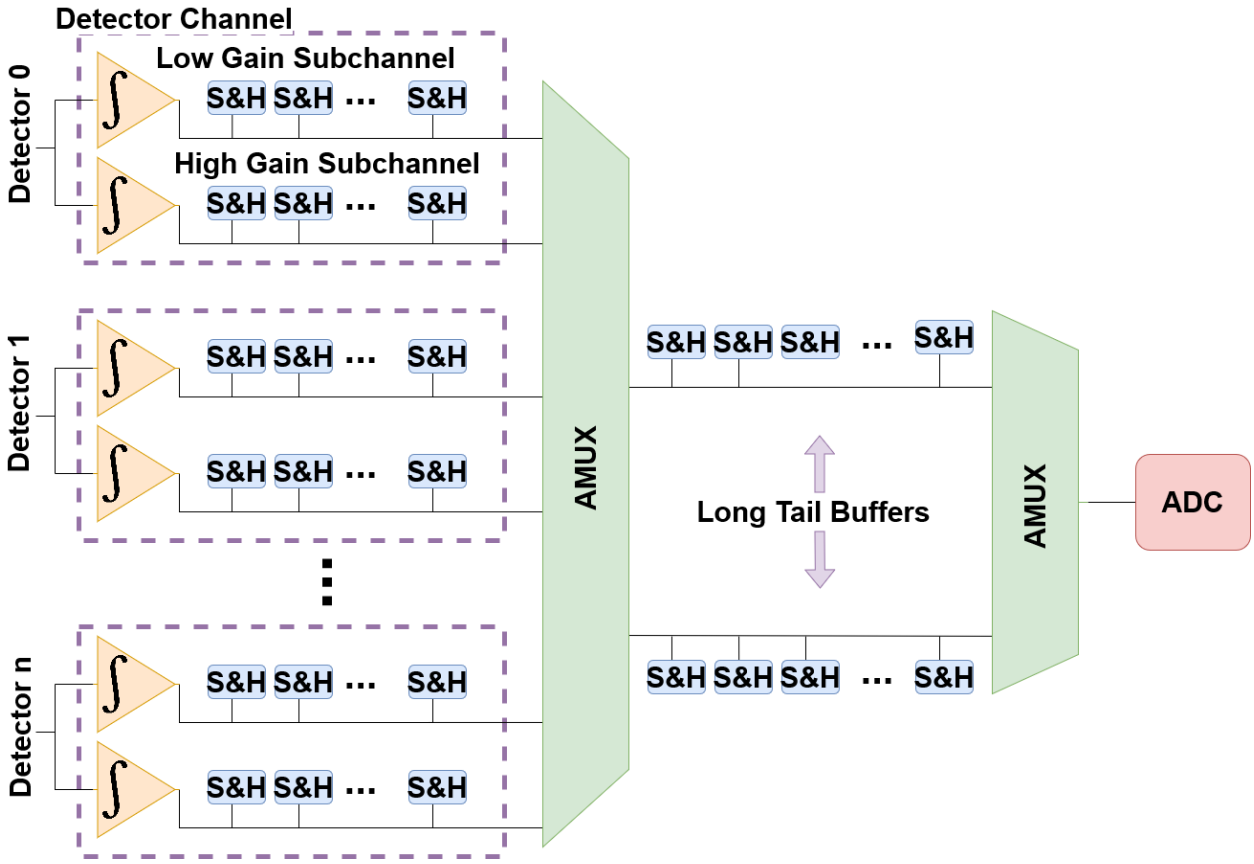

Figure 3.1: Block diagram of the proposed mixed-mode PSD system.

It is important to make sure the dead time between integral samples is minimized or else it will affect the PSD performance [1] since integral information will be missing between samples. This poses an issue since the integration capacitor will need to be reset to zero charge before each sample can be stored. To eliminate this problem our design uses a ping-pong integration circuit, shown in Figure 3.2, where each sub-channel has two integrators at the input so that while one integrator is resetting the other one can be integrating.

3.1.2 Long tail buffers

An external constant-fraction discriminator (CFD) circuit stops the continuous sampling into the short buffer for the triggered channel. The short buffer contents are retained and the channel begins sampling into one of a set of long tail buffers. A CFD is necessary since it

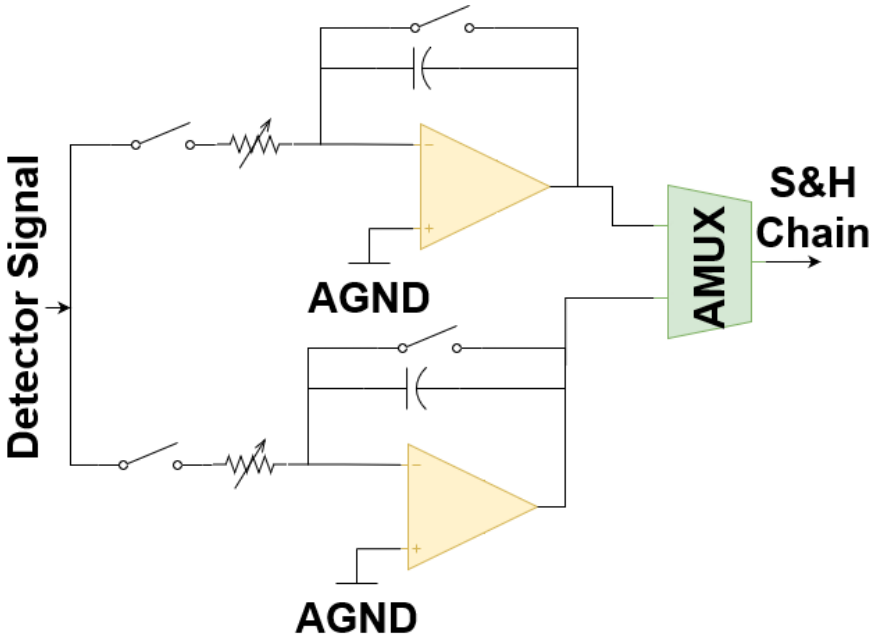

Figure 3.2: Ping-pong integrator circuit for eliminating inter-sample dead time. Each integrator block in Figure 3.1 is actually composed of this circuit.

provides an amplitude independent time reference [16] from which the peak time of the pulse can be inferred. From the peak time, the optimal late integration gate can be calculated. There are fewer long tail buffers than there are detector channels, so these act as shared hardware resources. Since it is unlikely that every single channel will be hit with radiation before a full chain of short and long buffers can be digitized, it makes sense to allocate these larger buffers as shared resources to maximize the number of detector channels integrated onto one chip.

Since the tail of the pulse, especially for neutrons, extends much further in time than the leading edge it is beneficial to have separate sample clocks for the short and long buffers. The long tail buffers use a much slower sample clock which allows each sample to correspond to a much longer integration period, allowing the total tail integral time region to be much longer. This could also be accomplished by using more sample and hold units but at the cost of integrated circuit die area and potentially leading to fewer detector channels supported on each chip.

3.2 Verilog-A Model

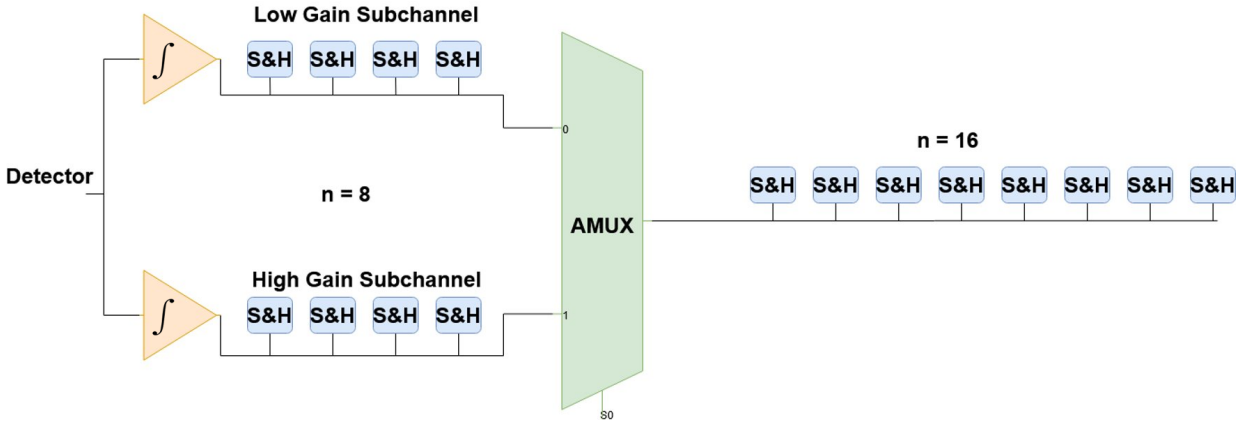

Figure 3.3: A single channel implementation of our mixed-mode PSD system. A short buffer size of 8 and a long buffer size of 16 sample and hold units were chosen respectively. The integrator blocks are each composed of the ping-pong integrator circuit from Figure 3.2.

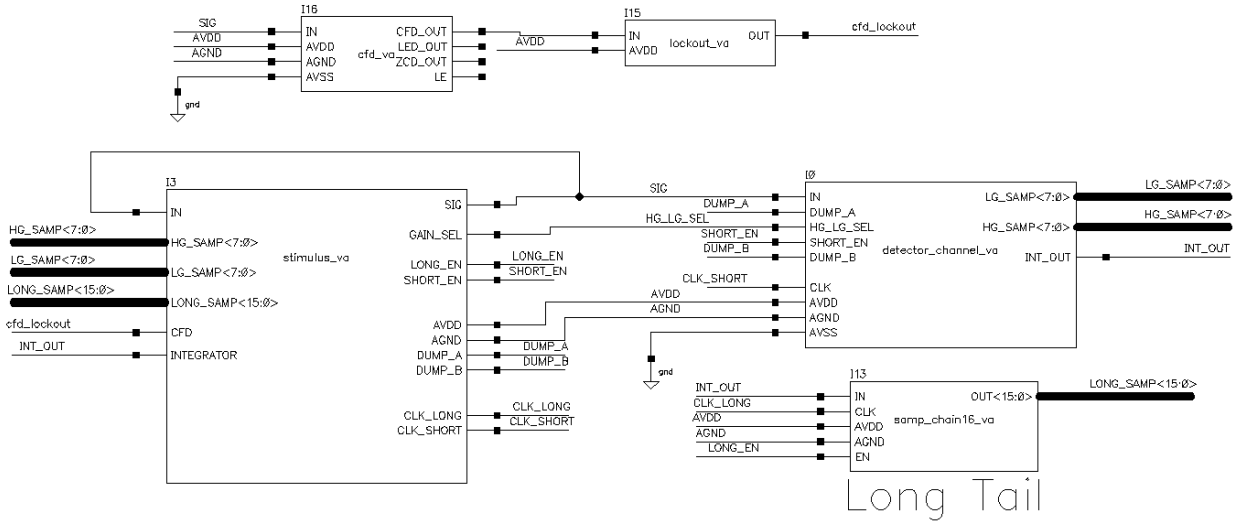

Figure 3.4: The single channel model in Cadence Virtuoso.

As a proof of concept we modeled a single channel, shown in Figure 3.3, of the proposed mixed-mode PSD system. The model, shown in Figure 3.4, is broken up into several independent Verilog-A models which were then connected as a circuit using the Cadence Virtuoso design tools. An external CFD circuit model was also created to act as the trigger and time reference. The control logic and input/output recording were all done with a single Verilog-A

block called `stimulus_va`. The Verilog-A code and other Cadence project files can be found at [11].

3.2.1 Detector channel model

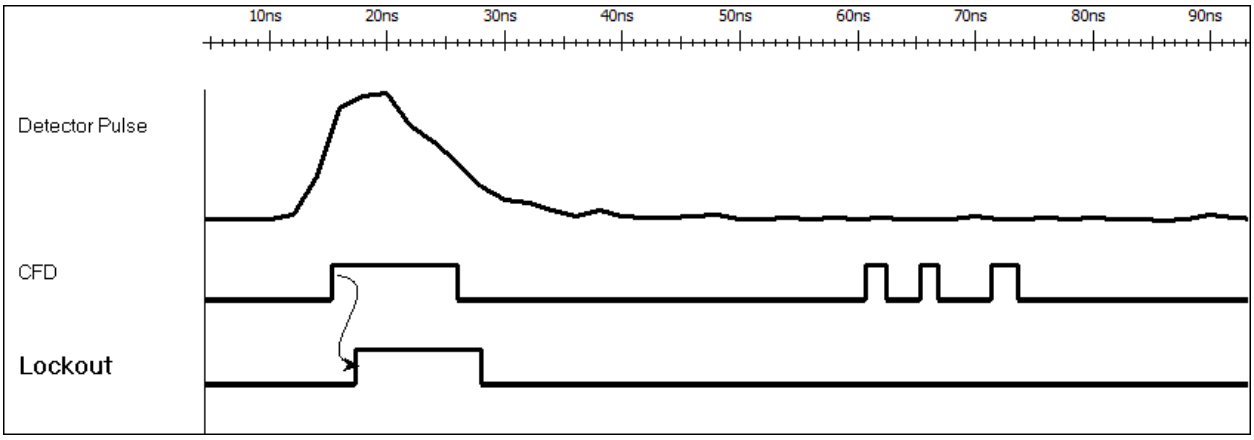

Figure 3.5: CFD lockout timing diagram. Notice that false CFD pulses are generated in the pulse tail from noise, but do not trigger the lockout oneshot used to trigger the signal channel.

The model hierarchy starts with a single detector channel model, CFD model, tail buffer model, and the `stimulus_va` block. The CFD model is coupled with a lockout oneshot model. This is because the noisy waveform data can cause false CFD triggers in the pulse tail so it is necessary to have a oneshot to suppress these false CFD events for some time [10]. The long tail buffer and short buffers use the same Verilog-A model but with a different number of sample and hold units. The CFD lockout logic is illustrated in Figure 3.5.

The sample and hold unit model is made to be ideal. An enable signal controls whether or not the sample and hold units respond to a clock edge. If it is enabled, then on each rising edge of the clock the voltage on the integrating capacitor is instantly recorded and stored in an array. The array values are converted to a voltage and provided via the output wires on the circuit block. The sample and hold unit control logic is illustrated in Figure 3.6.

The detector model block is broken up further by additional Verilog-A models for each sub-channel as shown in Figure 3.7. There is also an analog multiplexer (AMUX) model. The AMUX is modeled by a slew rate parameter and a single selection input wire. If the select

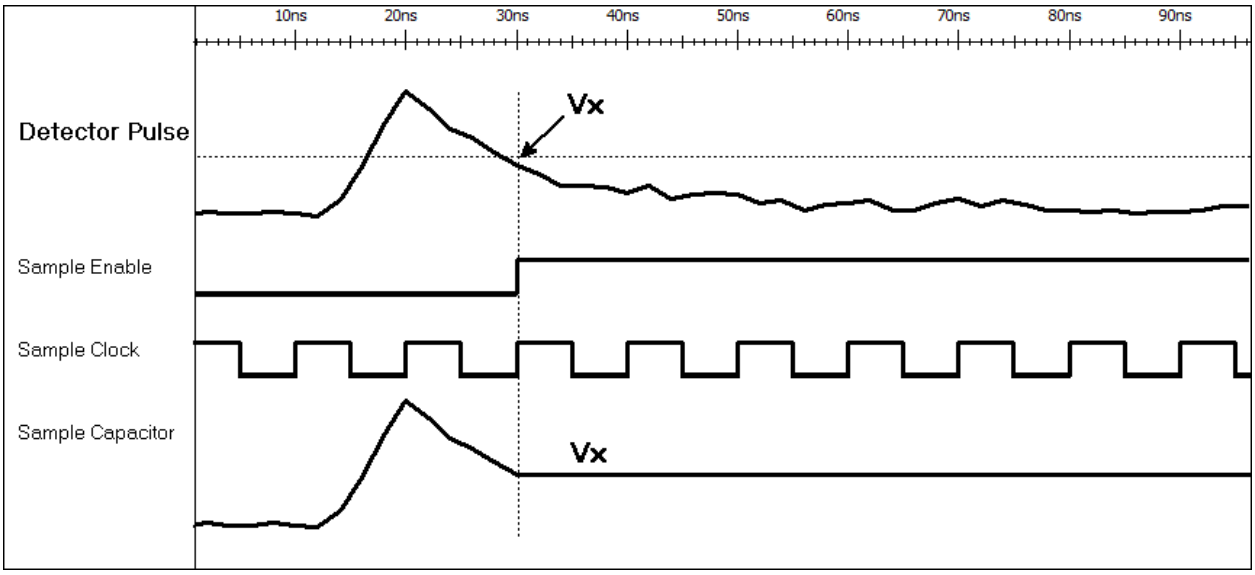

Figure 3.6: Each sample and hold cell has an enable singal that controls when hold is applied. If enabled, the next rising edge of the sample clock triggers a hold storing the voltage on the capacitor. The detector pulse is sampled here for illustration purposes, in actuality the output of an integrator is sampled.

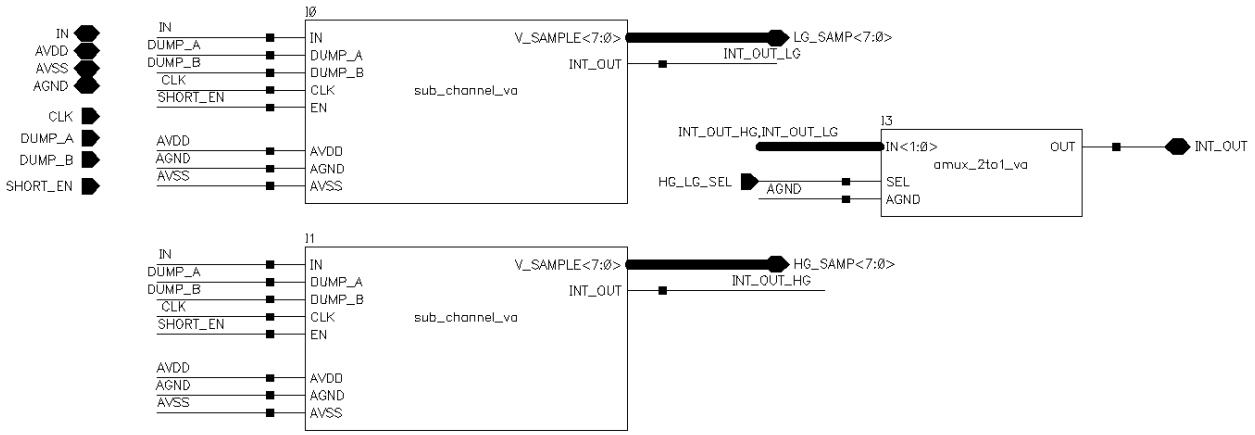

Figure 3.7: The detector channel model.

wire is above the logic threshold then the output changes at the slew rate to the voltage present on input 1, otherwise it changes at the slew rate to the voltage at input 0 as illustrated in Figure 3.8. The sub-channel models are identical only differing by the parameter values chosen for the integration resistor and capacitor.

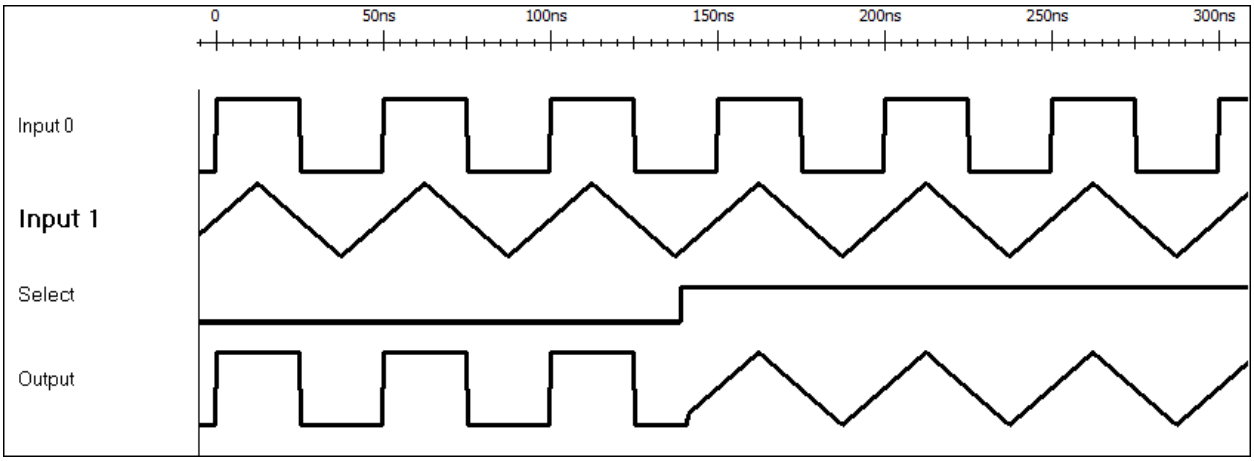

Figure 3.8: AMUX lockout timing diagram.

3.2.2 Sub-channel

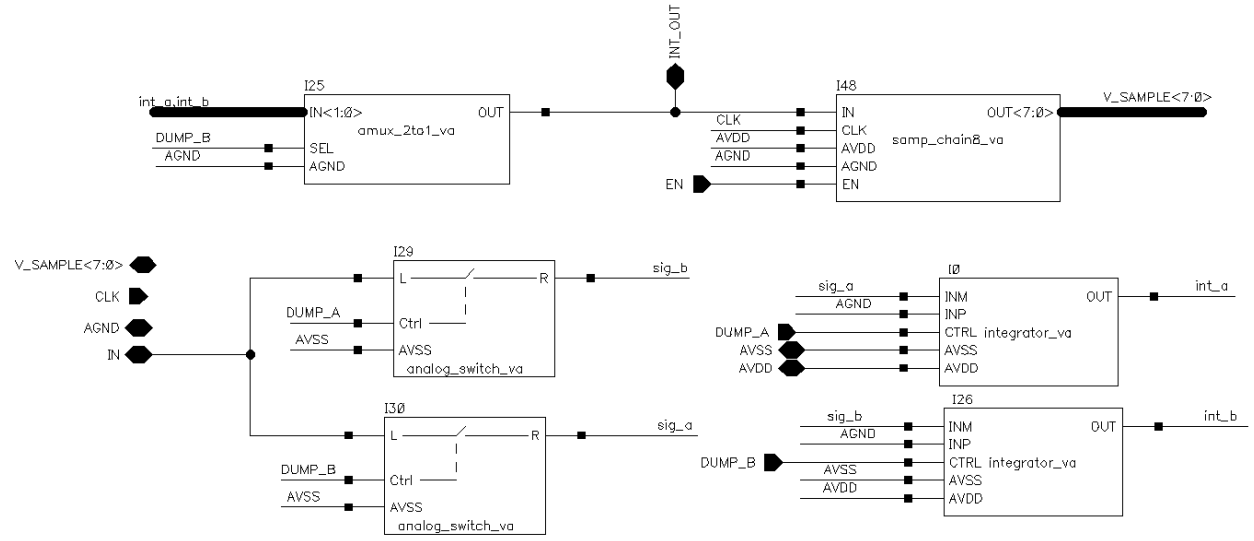

Figure 3.9: The Verilog-A models for a sub-channel.

The sub-channel model is shown in Figure 3.9. Each sub-channel is composed of an AMUX that is used to select which of the ping-pong integrators is being used for sampling, a pair of switches to control which integrator to send the input signal to, a pair of integrators that make up the ping-pong circuit, and the short buffer for that sub-channel. The switch models are modeled as a voltage controlled resistor. When the voltage is above the logic threshold the resistance of the switch transitions linearly to the on-resistance provided as a model

parameter. When it is below the logic threshold the switch transitions to the off-resistance parameter value. In our model we used an on-resistance of 100 Ω and an off-resistance of 1 GΩ.

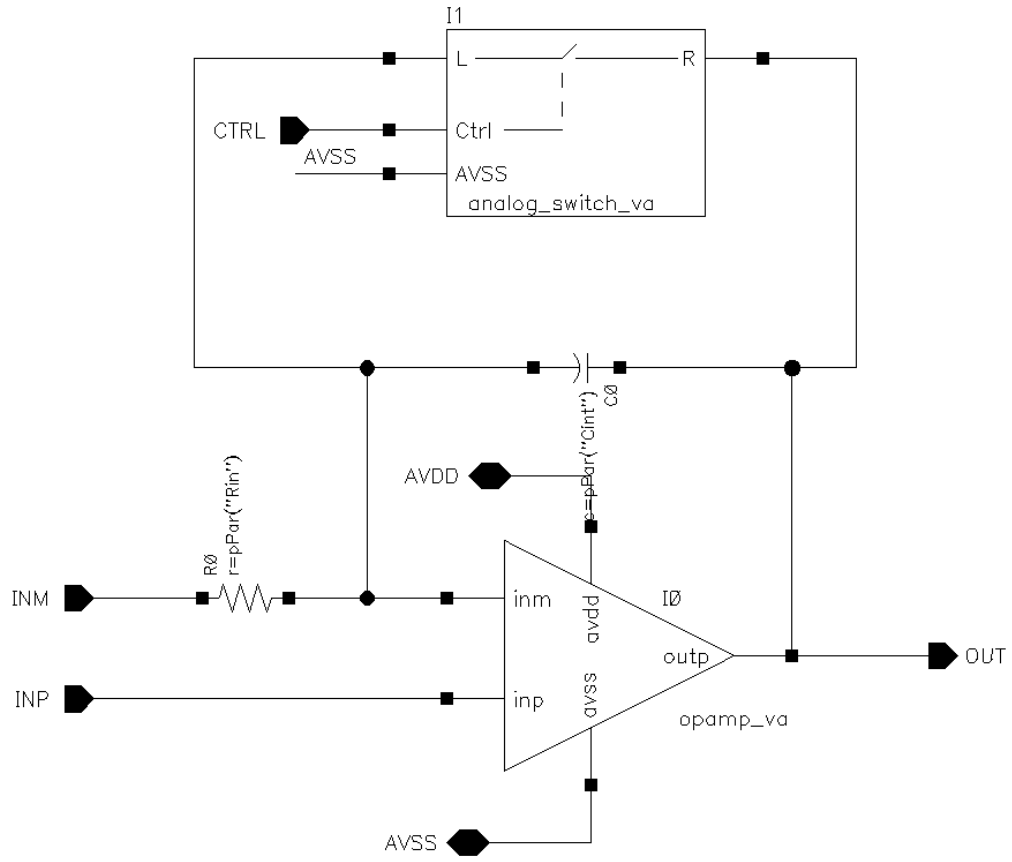

Figure 3.10: The Verilog-A models for an integrator.

The integrator block is shown in Figure 3.10. It is composed of a resistor, capacitor, Verilog-A opamp model, and a Verilog-A switch. The resistor and capacitors are SPICE models provided in our simulator's SPICE library. The switch model is used to reset the integrating capacitor when the dump signal is applied. The opamp is modeled in Verilog-A in the frequency domain using the inverse Laplace transform to create the output voltage. This is done via the `laplace_nd()` function in Verilog-A which allows a circuit to be modeled by two arrays which hold the coefficients for the numerator and denominator terms in a Laplace system equation. This allows an opamp to be modeled by

$$H(s) = \frac{\omega_u}{s + \omega_d} \tag{3.1}$$

where ω_u is the unity gain frequency and ω_d is the dominant pole. $H(s)$ in this case is the transfer function in the frequency domain. The `laplace_nd()` function call performs an inverse Laplace transform which is used to obtain the time domain output voltage of the opamp.

3.2.3 Model Verification

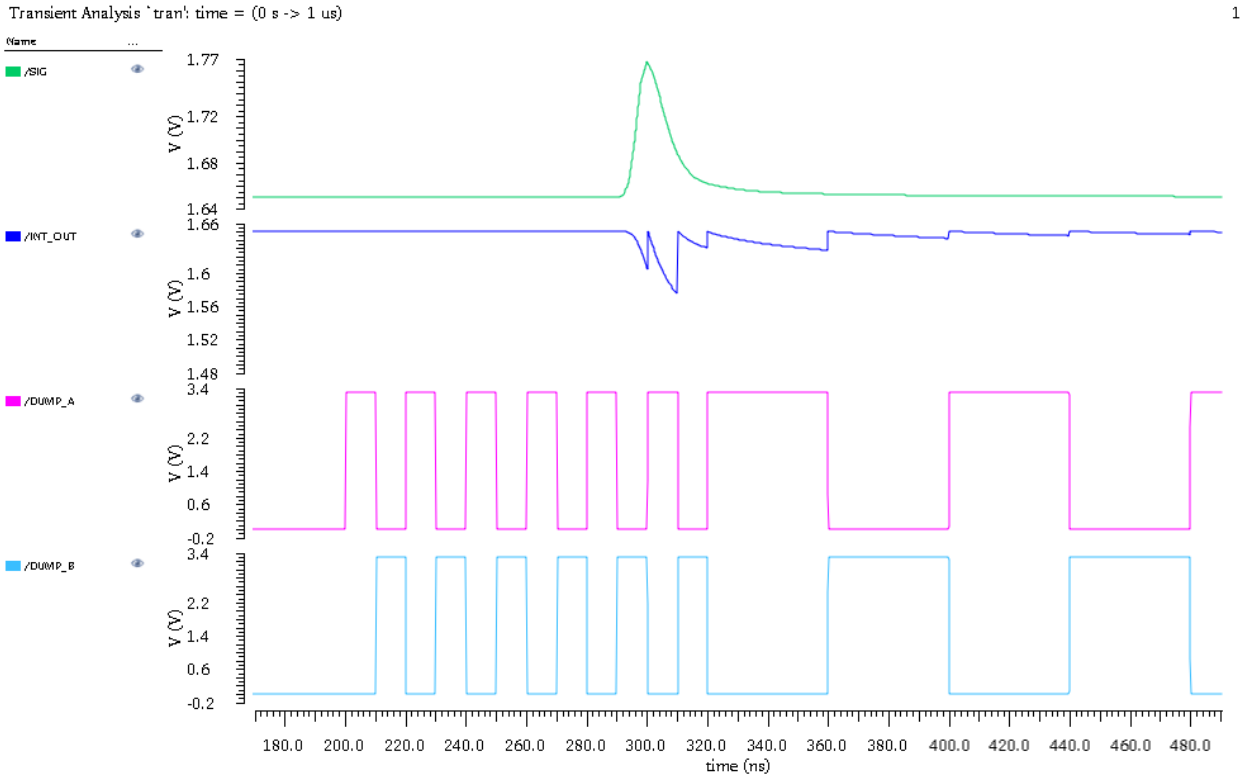

Figure 3.11: Spectre simulator output showing a functional ping-pong integrator circuit. Detector output shown in green, ping-pong integrator circuit output in blue, and the two integrator reset (i.e. DUMP) singals shown in magenta and cyan.

The full hierarchy of individual Verilog-A models combine to form a circuit that models a single channel of our mixed mode PSD design. Using the Spectre analog circuit simulator the

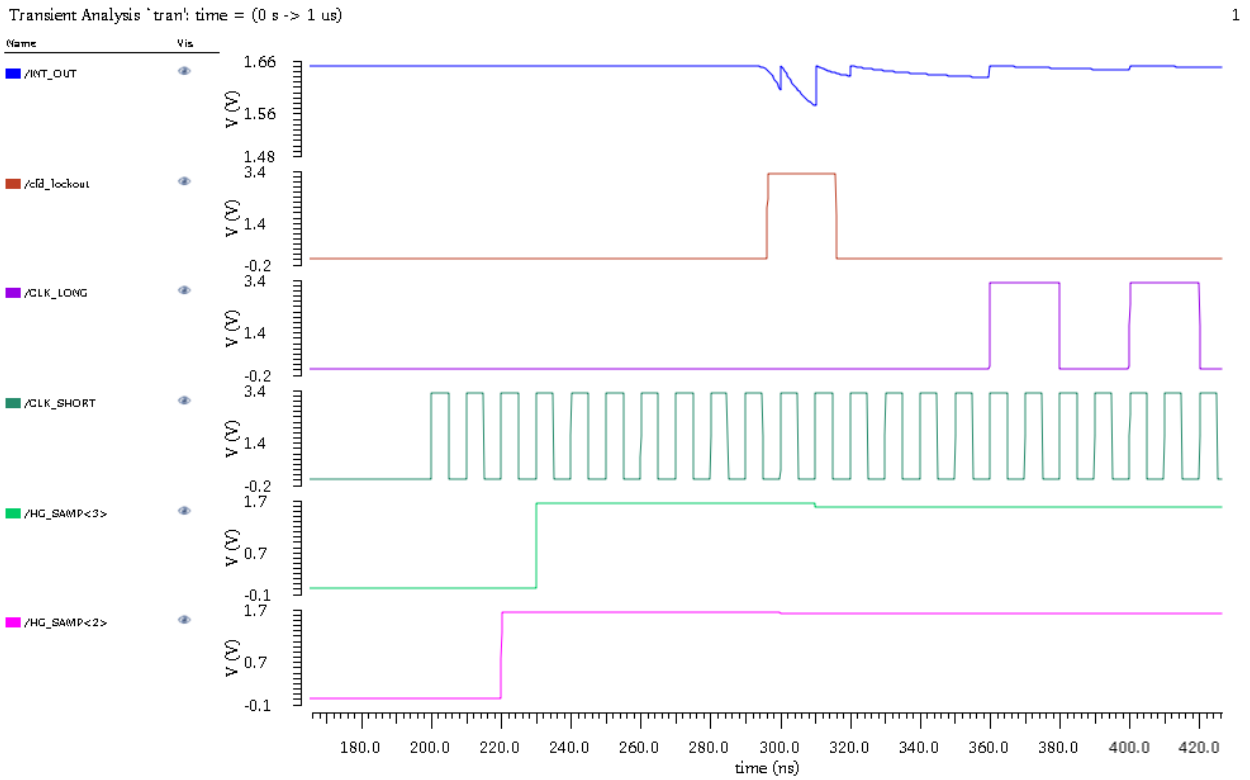

Figure 3.12: Spectre simulator output showing a functional control logic for storing integral samples. Ping-pong integrator outoput shown in blue, CFD trigger shown in brown, sample clock shown in green (short) and purple (long), and two sample capacitor outputs shown in magenta and light-green.

design was verified. The relevant waveform output can be seen in Figures 3.11 and 3.12 which shows that the model is functionally correct. Every rising edge a voltage sample is stored on the next sample capacitor. Every cycle the `DUMP_A` or `DUMP_B` alternate, selecting which ping-pong integrator is being used and which one is being reset. After the CFD signal two additional short samples are saved and the circuit transitions to longer integration periods for the tail buffers.

With a functional mixed-mode PSD model the performance of our design can be analyzed. In the next chapter analysis of more detailed simulations is given, including quality metrics by which the discrimination performance of our model can be determined.

Chapter 4

Results

In order to verify that our mixed-mode system is PSD capable we need to use real waveform data from actual scintillators as input to our Verilog-A models. Using the single channel model depicted in Figure 3.3 and experimental scintillator data from [18] we set out to test our system model. A short buffer length of 8 and long buffer length of 16 were chosen, and their corresponding sample periods of 10 ns and 40 ns respectively were used. These values were not determined to be optimal but were instead chosen as reasonable values for capturing pulse-shape information from our dataset. The dataset contains pulse data from real sampled (at 500 MSPS) scintillator waveforms from several different scintillators each with slightly different properties. The waveform sample points were turned into analog waveforms for our Verilog-A models by performing interpolation of the points in a piece-wise linear fashion.

4.1 PSD Simulations

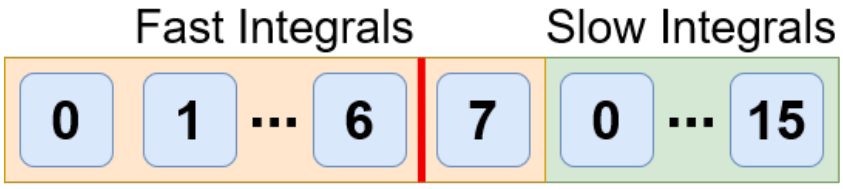

Figure 4.1: Early/late integrals saved in the short and long buffers. To the right of the red line are late integrals; to the left are early integrals.

Simulations were run using 17,500 pulses from BC501A and P-terphenyl scintillators with the CCM algorithm being used for generation of the discriminating parameter D. For the

proposed system the CCM algorithm works by drawing a boundary between *early integrals* and *late integrals* (see Figure 4.1) and defining the discriminating variable by

$$D = \frac{\sum_{i=c+k}^{7} S_i + \sum_{i=0}^{15} L_i}{\sum_{i=0}^{7} S_i + \sum_{i=0}^{15} L_i} \tag{4.1}$$

where c is the index of the first sample after the CFD trigger, k is the optimal number of early integral samples to save after the trigger, and S_i and L_i denote the ith sample in the short and long buffers respectively. The numerator of equation 4.1 is the sum of all of the late integral samples while the denominator is the total sum of all integral samples. The advantage of defining D this way is that the system can be configured with a different value for k for each experiment, since each scintillator has slightly different optimal late integration times [18]. After simulating all of the waveforms the resulting plots (Figure 4.2 and Figure 4.3) for D vs energy shows clear ability to discriminate between gamma rays and neutrons for both BC501A and P-terphenyl. Notice that Figure 4.2 looks very similar to Figure 2.3, showing that our mixed-mode PSD system performs very similarly to state of the art DSP based systems.

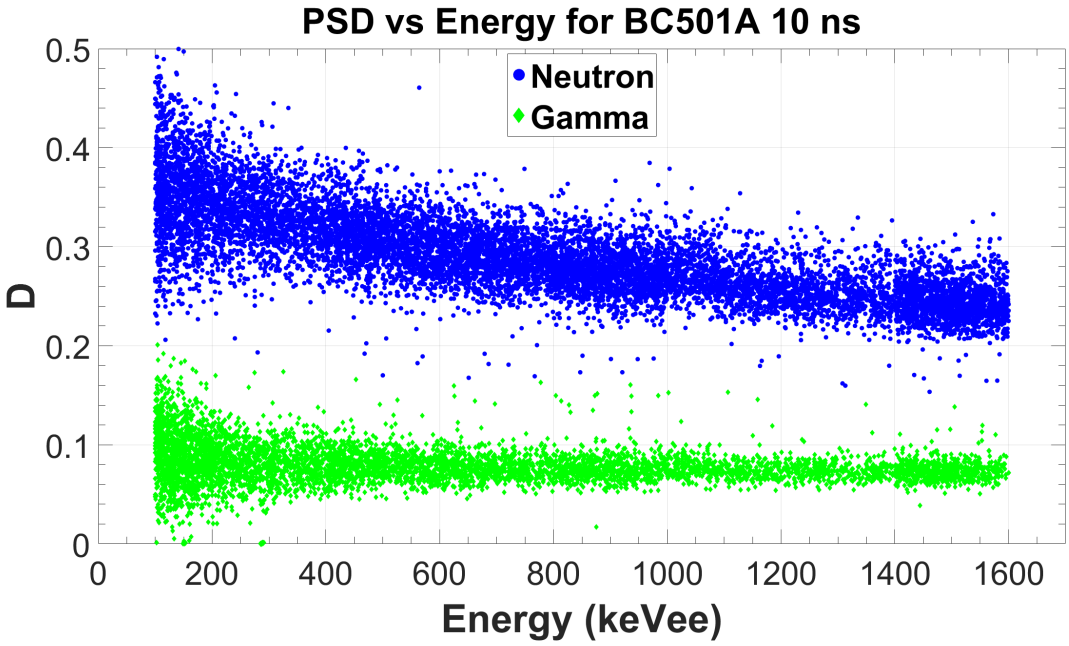

Figure 4.2: n/γ discrimination in BC501a using our mixed-mode PSD models.

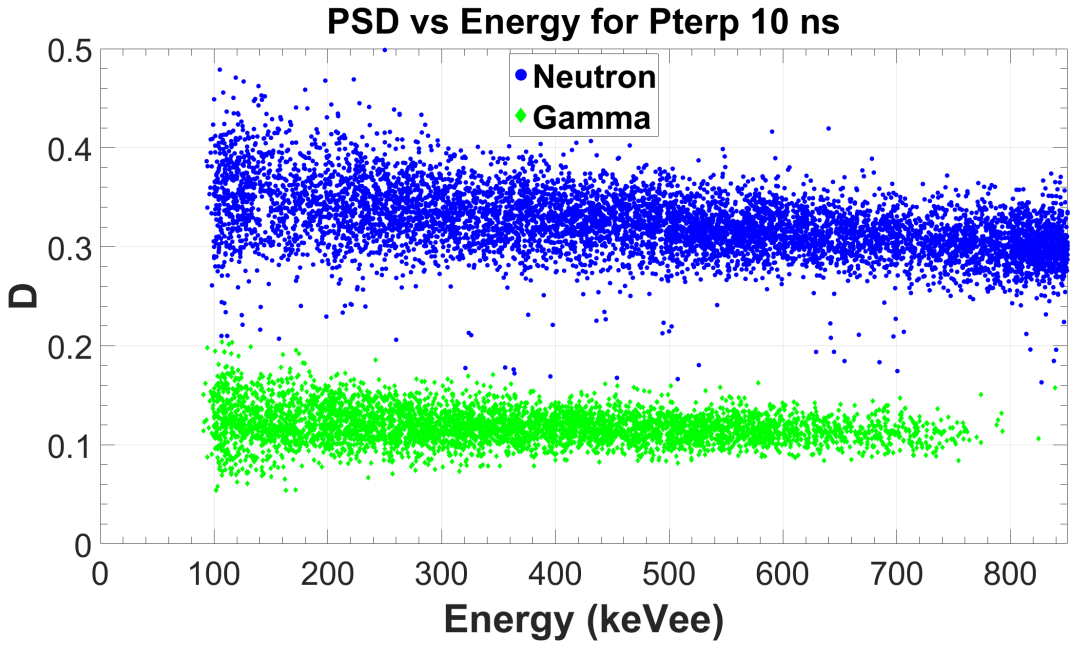

Figure 4.3: n/γ discrimination in P-terphenyl using our mixed-mode PSD models.

4.2 Quality Metrics

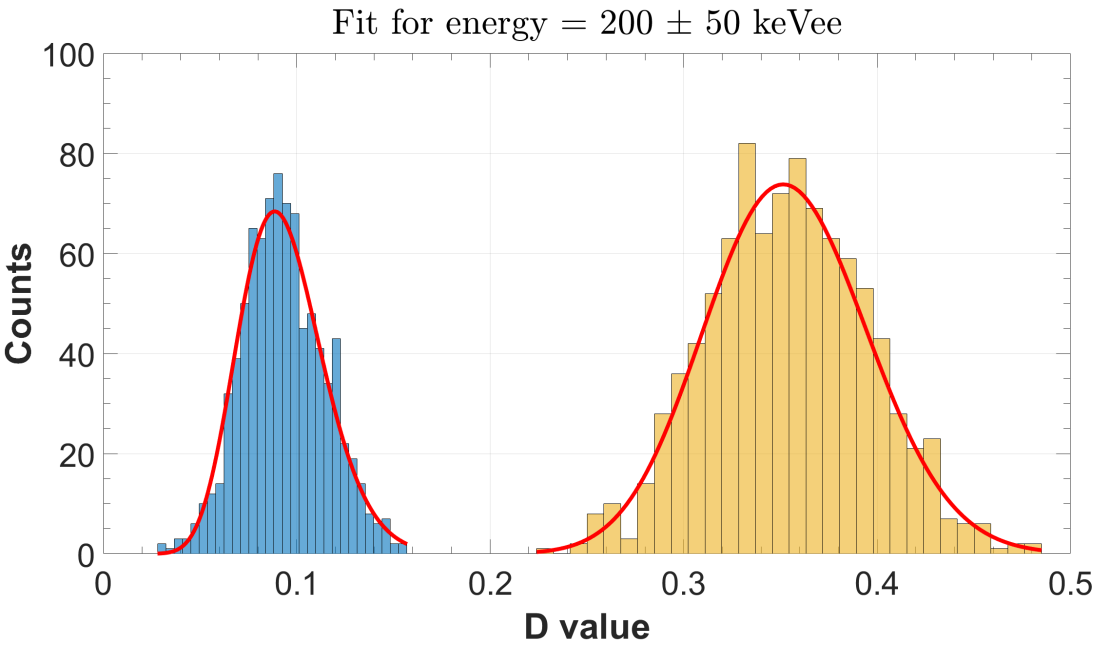

Figure 4.4: Distribution of D over the energy range 150-250 keVee for BC501A.

While Figures 4.2 and 4.3 clearly show that our mixed mode PSD system is capable of discriminating between radiation types, it does not easily convey how well it is discriminating. In order to quantify this a commonly used figure of merit (FOM) was used [8]. This FOM is obtained by analyzing the distribution of D over narrow energy ranges. This produces a bimodal histogram as shown in Figure 4.4, where each mode is a different type of radiation (i.e. neutron or gamma ray). From this distribution the FOM is calculated by

$$\text{FOM} = \frac{|\mu_n - \mu_\gamma|}{\text{FWHM}_n + \text{FWHM}_\gamma} \tag{4.2}$$

where μ_n and μ_γ are the means of a skewed Gaussian fit over the neutron and gamma distributions respectively, and FWHM_n and FWHM_γ are the full widths at half maximums. This FOM encapsulates two quality metrics: the distance between the peaks of each mode, and how spread out each mode is. A higher FOM value corresponds to better discrimination capabilities. Using this metric we plotted the FOM vs energy for our mixed-mode system and compared it to state of the art DSP based systems, achieving similar results. Figures 4.5 and 4.6 show the results of this exercise for BC501A and P-terphenyl respectively.

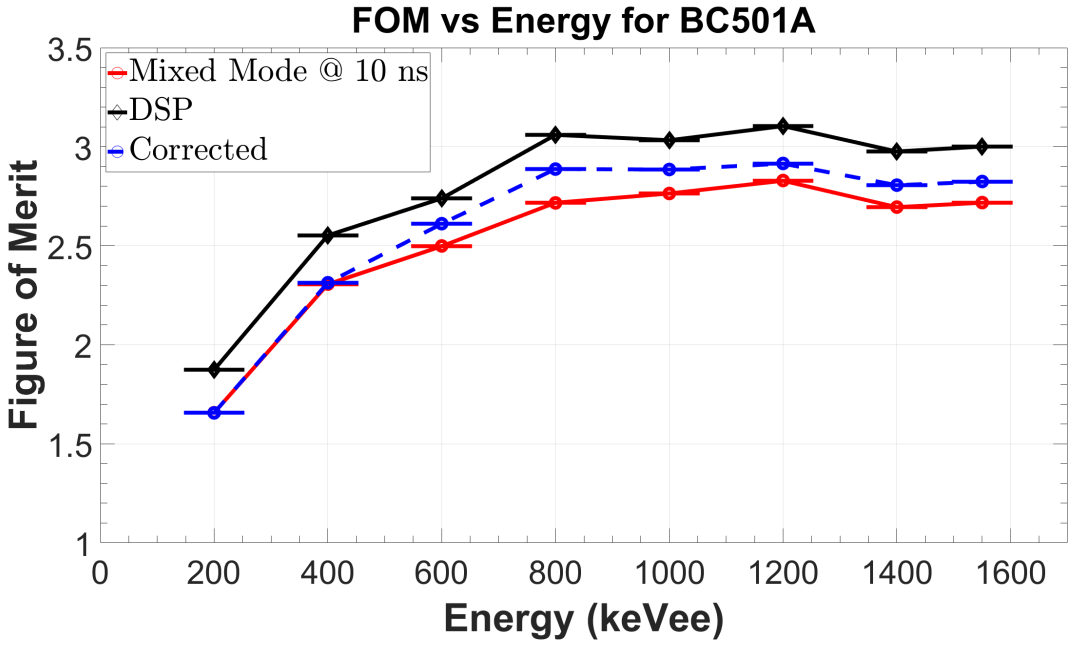

Figure 4.5: FOM for BC501A showing our mixed-mode PSD system (solid red), traditional DSP methods (solid black), and mixed-mode PSD after phase correction (dashed blue).

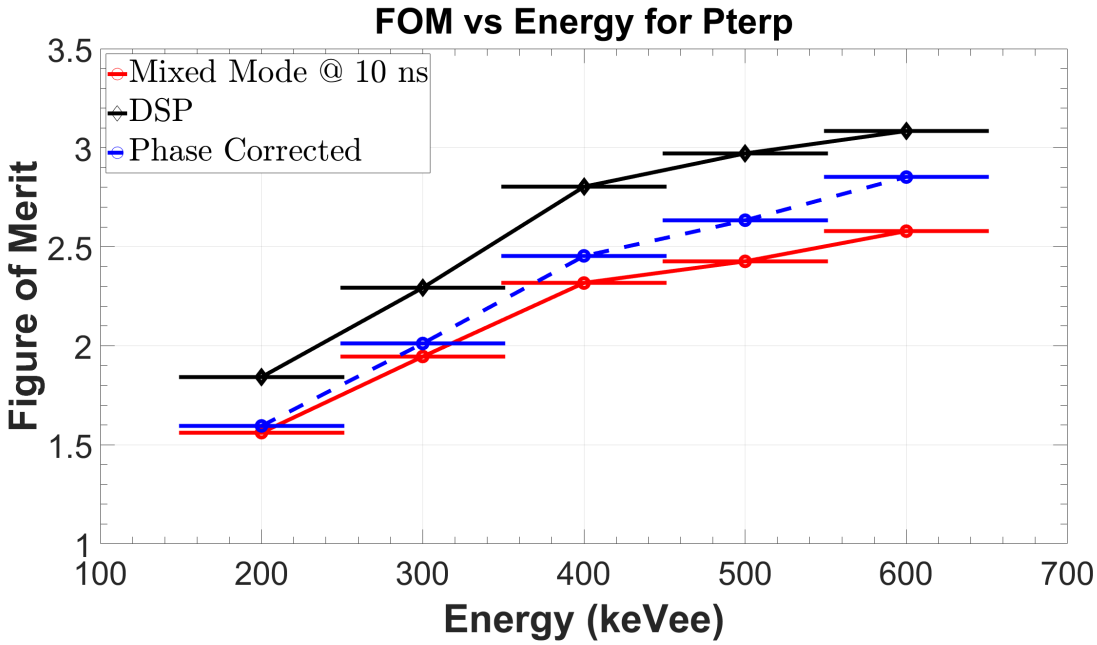

Figure 4.6: FOM for P-terphenyl showing our mixed-mode PSD system (solid red), traditional DSP methods (solid black), and mixed-mode PSD after phase correction (dashed blue).

4.3 Phase Error Correction

One potential issue with this mixed-mode PSD topology is that the detector waveform pulse is entirely asynchronous to the sample clock. This means that the detector pulse will have some phase delay relative to the sample clock. This is important because the optimal start time of the late integration gate is defined with respect to the sample peak. This introduces some potential phase error into the optimal late integral gate time with our system, the effect of which can be seen in Figure 4.7. To compensate for this phase error a simple linear interpolation algorithm (Figure 4.8) was used on the two samples on the boundary of the late and early integrals. To give better time resolution, k was chosen such that a sample on either side of the optimal boundary would be in the short buffer.

Using the CFD time as a reference time the optimal late integration boundary is calculated. If this boundary does not fall on a rising edge of the sample clock the linear interpolation algorithm is used to compensate. The algorithm interpolates a line between the two samples that are separated by the boundary and then computes a new value for each of these samples

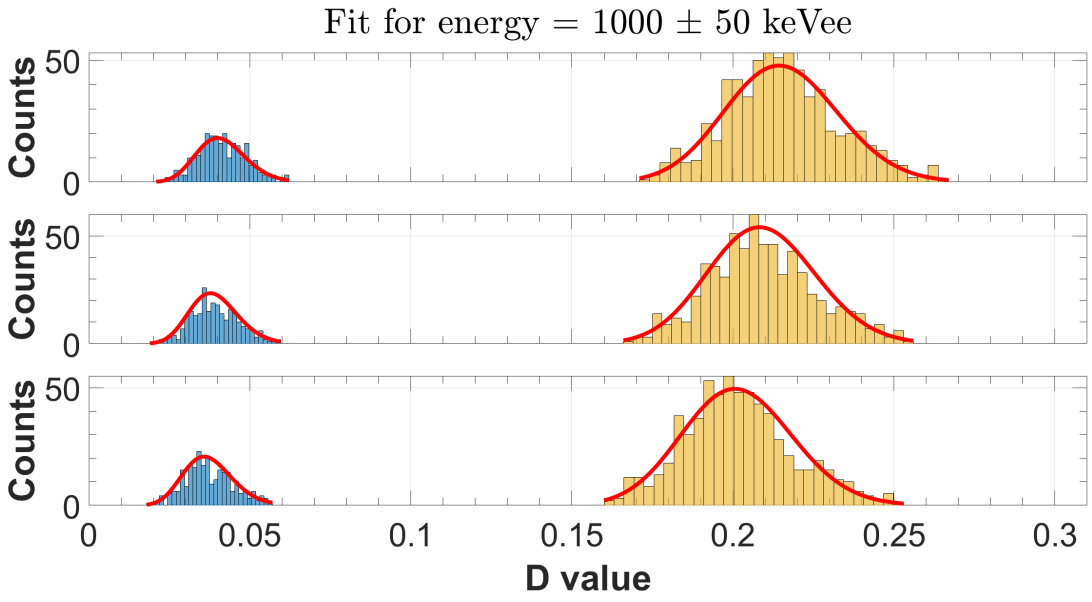

Figure 4.7: Effect of phase error on distribution of D showing +3 ns error (top), no phase error (middle), and -3 ns phase error (bottom).

by shifting them along this line by the phase difference between the CFD trigger and sample clock.

For BC501A the results were underwhelming with under 3% improvement in the FOM on average over the entire energy range. However as can be seen in Figure 4.6(b) the p-terphenyl scintillator is more responsive to this method with an average of 6% improvement across the entire energy range. This indicates that the ability to correct for phase error is scintillator dependent, and different algorithms may be better suited to different scintillators. Phase error correction also becomes more important as sample clock rates get slower, since there is more time between each clock edge in which the CFD pulse can come. Because of this phase correction is likely more important on slower scintillators with rise times of hundreds of nanoseconds or more.

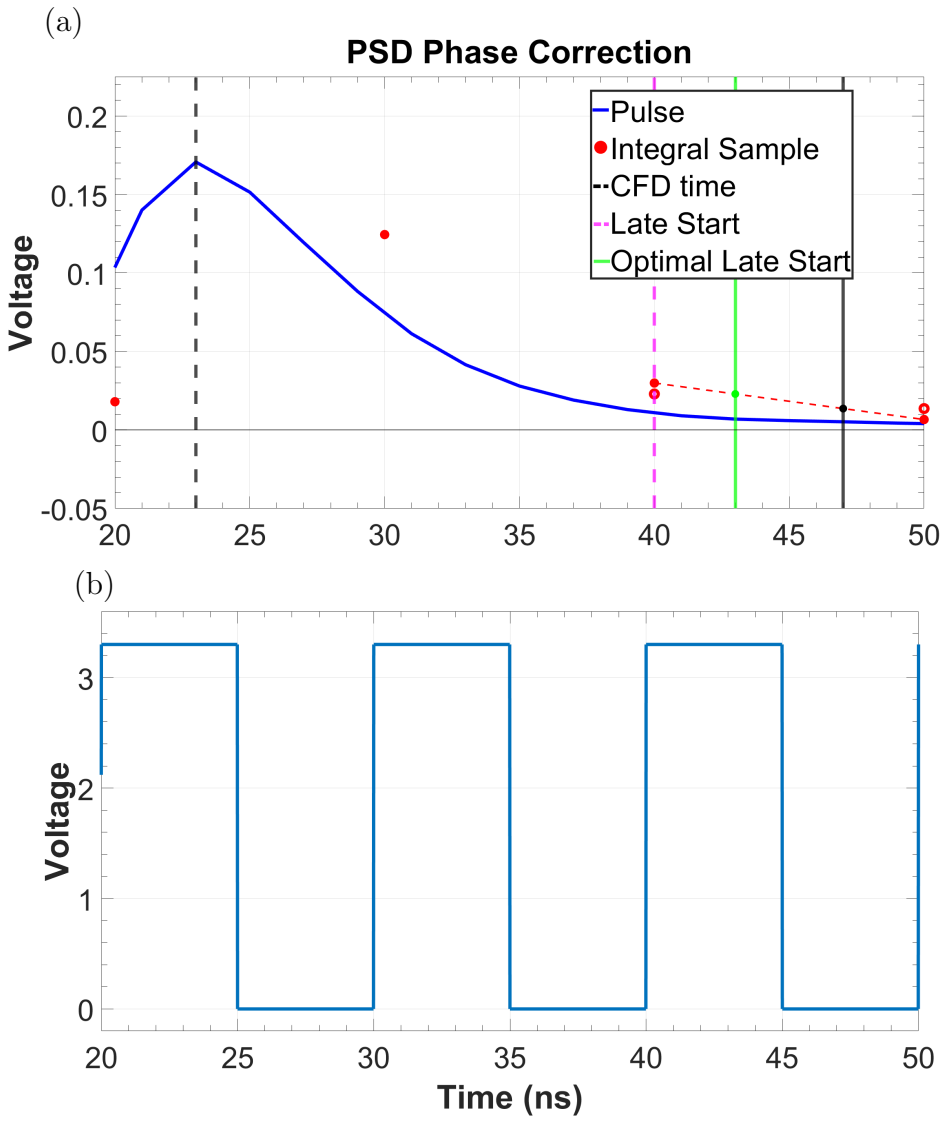

Figure 4.8: Phase correction using linear interpolation (a) and sample clock (b). Open circles indicate new integral sample values after phase correction.

Chapter 5

Conclusion and Future Work

In this work an integrated circuit topology for a mixed-mode PSD system is proposed. This mixed-mode topology consists of analog circuitry presented in a manner that lends its self to DSP algorithms. This is done by doing some pulse processing in hardware via hardware integrators, but taking many small integrals and storing them in analog memory. This allows the system to get all of the necessary pulse-shape information without needing hundreds of samples. It also allows for slow digitizers since samples are stored in memory, making the system cost comparable to that of traditional analog PSD ASICs.

By modeling this circuitry in Verilog-A and using real detector data as the input to our models we showed that the mixed-mode PSD topology offers similar performance to state of the art DSP based systems. Additionally, since the system consists of simple analog circuitry it is possible to build high density integrated circuits for large channel count detectors. It is also possible to correct for phase errors that are inherent in this design using simple DSP algorithms. And while not tested in this work, it is worth noting that algorithm flexibility is maintained with this mixed-mode topology. For example, pile-up events can be detected by observing the monotonicity of the integral samples in the tail since in a pile-up event there will be two peaks which will result in sudden spikes in the integral output in the tail region above the noise level.

The purpose of this work is to show that a mixed-mode PSD ASIC is viable and could offer advantages over pure analog systems and DSP based systems. To build upon this work a formal optimization of the integrated circuit parameters could be done. The number of sample and hold units and number of long tail buffers were not chosen optimally in this work. A formal optimization would allow for a selection of these values that would maximize the

number of detector channels supported by a single ASIC, minimize the probability of missing an event, and maximizing the dynamic range to give better discrimination capabilities.

Following a formal optimization the integrated circuit could be designed with the optimal parameters in mind. This design would entail the complete transistor level design and layout of the various circuits needed for the system such as the integrators, sample and hold units, analog multiplexers, and control logic. The circuit-level designs would be simulated with the same real world data used in this work to verify the functionality and performance of the design using real transistor level implementations. Once the design is verified a real integrated circuit chip could be fabricated and tested against the simulated performance.

After fabrication the mixed-mode PSD chips could then be used in a real world experiment. This would be the real test to show whether or not a mixed-mode PSD system offers advantages over analog and DSP counterparts. Using real experimental data the system could be compared to the state of the art not just in terms of its performance as a waveform digitizer, but also in terms of it's ability to augment nuclear science research in ways that were previously inaccessible.

References

[1] Leonardo Abbene and Gaetano Gerardi. High-rate dead-time corrections in a general purpose digital pulse processing system. *Journal of Synchrotron Radiation*, 22(5):1190–1201, Sep 2015.

[2] R. Aryaeinejad, J.K. Hartwell, and D.F. Spencer. Comparison between digital and analog pulse shape discrimination techniques for neutron and gamma ray separation. In *IEEE Nuclear Science Symp. Conf. Record*, volume 1, pages 500–504, 2005.

[3] Francesco Belli, Basilio Esposito, Daniele Marocco, and Marco Riva. A study on the pulse height resolution of organic scintillator digitized pulses. *Fusion Engineering and Design*, 88(6):1271–1275, 2013. Proceedings of the 27th Symposium On Fusion Technology (SOFT-27); Liège, Belgium, September 24-28, 2012.

[4] G.L. Engel, N. Duggireddi, V. Vangapally, J.M. Elson, L.G. Sobotka, and R.J. Charity. Multi-channel integrated circuits for the detection and measurement of ionizing radiation. *Nucl. Instr. and Meth. A*, 652(1):462–465, 2011.

[5] G.L. Engel, M.J. Hall, J.M. Proctor, J.M. Elson, L.G. Sobotka, R. Shane, and R.J. Charity. Design and performance of a multi-channel, multi-sampling, PSD-enabling integrated circuit. *Nucl. Instr. and Meth. A*, 612(1):161–170, 2009.

[6] Michael J. Hall. Design considerations in systems employing multiple charge integration for the detection of ionizing radiation. Master's thesis, Southern Illinois University Edwardsville, December 2007.

[7] T. A. King and R. Voltz. The time dependence of scintillation intensity in aromatic materials. *Proceedings of the Royal Society of London. Series A, Mathematical and Physical Sciences*, 289(1418):424–439, 1966.

[8] W. G. J. Langeveld, M. J. King, J. Kwong, and D. T. Wakeford. Pulse shape discrimination algorithms, figures of merit, and gamma-rejection for liquid and solid scintillators. *IEEE Trans. on Nuclear Science*, 64(7):1801–1809, 2017.

[9] M. Nakhostin. Digital discrimination of neutrons and γ-rays in liquid scintillation detectors by using low sampling frequency adcs. *Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment*, 916:66–70, 2019.

[10] Bryan Orabutt. Design and analysis of a multi-channel discriminator integrated circuit for use in nuclear physics experiments. Master's thesis, Southern Illinois University Edwardsville, August 2018.

[11] Bryan Orabutt. Cadence design files. `https://github.com/BryanOrabutt/mm-psd-design`, 2021.

[12] Bryan Orabutt. MATLAB Source code. `https://github.com/BryanOrabutt/mixed-mode-psd`, 2021.

[13] Bryan Orabutt, Roger D. Chamberlain, Jonathan Elson, George Engel, Franck Delaunay, and Lee G. Sobotka. Design of mixed-mode systems for pulse-shape discrimination. In *2021 IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pages 990–994, 2021.

[14] Justin M. Proctor. Design of a multi-channel integrated circuit for use in nuclear physics experiments where particle identification is required. Master's thesis, Southern Illinois University Edwardsville, December 2007.

[15] Stefan Ritt. Design and performance of the 6 GHz waveform digitizing chip DRS4. In *2008 IEEE Nuclear Science Symposium Conference Record*, pages 1512–1515, 2008.

[16] J.-M. Régis, M. Rudigier, J. Jolie, A. Blazhev, C. Fransen, G. Pascovici, and N. Warr. The time-walk of analog constant fraction discriminators using very fast scintillator detectors with linear and non-linear energy response. *Nucl. Instr. and Meth. A*, 684:36–45, 2012.

[17] C.S. Sosa, M. Flaska, and S.A. Pozzi. Comparison of analog and digital pulse-shape-discrimination systems. *Nucl. Instr. and Meth. A*, 826:72–79, 2016.

[18] M. Sénoville, F. Delaunay, M. Pârlog, N.L. Achouri, and N.A. Orr. Neutron-γ discrimination with organic scintillators: Intrinsic pulse shape and light yield contributions. *Nucl. Instr. and Meth. A*, 971:164080, 2020.

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